Electronic Version

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Claims

[c1] An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET) wherein a first strain is applied to the channel region of the PFET but not the NFET via a semiconductor layer disposed in source and drain regions of the PFET and not of the NFET, said semiconductor layer being lattice-mismatched to a single-crystal semiconductor disposed in said channel regions of said PFET and said NFET.

[c2] The integrated circuit of claim 1 wherein channel regions of said PFET and said NFET are disposed in a single-crystal region of a first semiconductor and said lattice-mismatched semiconductor includes a layer of a second semiconductor disposed over said single-crystal region of said first semiconductor.

[c3] The integrated circuit of claim 2 wherein said single-crystal region of said first semiconductor has a main surface defined by a level of a gate dielectric of a gate stack of said PFET and said layer of said second semiconductor has a top surface disposed beneath said main

surface.

[c4] The integrated circuit of claim 3 further comprising a single-crystal layer of said first semiconductor disposed over said layer of said second semiconductor.

[c5] The integrated circuit of claim 1 wherein said first semiconductor consists essentially of a semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide and said second semiconductor consists essentially of another semiconductor different from said first semiconductor, said another semiconductor selected from the group consisting of silicon, silicon germanium and silicon carbide.

[c6] The integrated circuit of claim 1 wherein said first semiconductor consists essentially of silicon and said second semiconductor consists essentially of silicon germanium.

[c7] The integrated circuit of claim 1 wherein said first semiconductor consists essentially of silicon germanium according to a first formula $Si_{x1}Ge_{y1}$, where x1 and y1 are percentages, $x1 + y1 = 100\%$, y1 being at least one percent and said second semiconductor consists essentially of silicon germanium according to a second formula $Si_{x2}Ge_{y2}$, where x2 and y2 are percentages, $x2 + y2 = 100\%$, y2 being at least one percent, wherein x1 is not

equal to x2 and y1 is not equal to y2.

[c8] The integrated circuit of claim 1 wherein said first strain is a compressive strain.

[c9] The integrated circuit of claim 6 wherein said second semiconductor consists essentially of silicon germanium having a germanium content of at least one percent.

[c10] The integrated circuit of claim 4 wherein each of said PFET and said NFET further comprise a layer of silicide contacting gate conductors, source regions and drain regions of said PFET and said NFET.

[c11] The integrated circuit of claim 10 wherein said silicide consists essentially of a silicide of cobalt.

[c12] An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET) each having channel regions disposed in single-crystal silicon regions of a substrate wherein a first strain is applied to the channel region of the PFET but not the NFET via a buried lattice-mismatched semiconductor layer consisting essentially of silicon germanium disposed in source and drain regions of the PFET and not of the NFET, said silicon germanium having proportions according to the formula Si_xGe_y where x and y

are percentages each being at least one percent, x plus y equaling 100 percent.

[c13] A method of fabricating a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), said NFET and said PFET each having a channel region, said channel region of said PFET having a first strain and said channel region of said NFET not having said first strain, said method comprising:
forming a PFET gate stack and an NFET gate stack over a main surface of a single-crystal region of a first semiconductor, each of said PFET gate stack and said NFET gate stack including a gate dielectric, a gate conductor formed thereon, a cap layer formed over said gate conductor and first spacers formed on sidewalls of said gate conductor;
recessing said single-crystal region on sides of said PFET gate stack while protecting said main surface of said single-crystal region on sides of said NFET gate stack from being recessed;
growing a layer of a second semiconductor in areas of said single-crystal region exposed by said recessing while preventing said layer from growing on said single-crystal region on sides of said NFET gate stack, said second semiconductor being lattice-mismatched to said first semiconductor to apply said first strain to said

channel region of said PFET; and

fabricating source and drain regions on said sides of said PFET gate stack to form said PFET and fabricating source and drain regions on said sides of said NFET gate stack to form said NFET.

[c14] The method of claim 13 further comprising recessing said layer of second semiconductor below said main surface of said single-crystal region.

[c15] The method of claim 14 further comprising growing a layer of said first semiconductor over said recessed second semiconductor layer.

[c16] The method of claim 15 further comprising forming a self-aligned silicide (salicide) over said source and drain regions of said PFET and of said NFET.

[c17] The method of claim 16 further comprising forming a self-aligned silicide (salicide) over polysilicon portions of said gate conductors of said PFET and said NFET.

[c18] The method of claim 17 wherein said silicide includes a silicide of cobalt

[c19] The method of claim 15 wherein said first semiconductor comprises silicon and said second semiconductor comprises silicon germanium, said silicon germanium having

a germanium content of at least one percent.

[c20] The method of claim 19 wherein said lattice-mismatched second semiconductor applies a compressive strain to said channel region of said PFET.

[c21] The method of claim 13 wherein said step of forming said source regions and drain regions further includes removing said first spacers from said PFET gate stack and said NFET gate stack and forming second spacers on sidewalls of said PFET gate stack and said NFET gate stack.

[c22] The method of claim 21 wherein said second spacers have a greater thickness than said first spacers.

[c23] The method of claim 21 further comprising halo implanting exposed areas of said single-crystal region and said layer of said first semiconductor.

[c24] The method of claim 21 further comprising extension implanting exposed areas of said single-crystal region and said layer of said first semiconductor.

[c25] The method of claim 22 further comprising forming third spacers laterally contacting said second spacers, and implanting source and drain regions in said exposed areas of said single-crystal region and said layer of said first

semiconductor.

[c26] The method of claim 13 wherein said single-crystal region on said sides of said NFET gate stack are prevented from being recessed by a patterned block mask.

[c27] The method of claim 13 wherein said second semiconductor layer is prevented from growing on said single-crystal region on said sides of said NFET gate stack by applying a first coating to said single-crystal region on said sides of said NFET gate stack.

[c28] The method of claim 27 wherein said coating is formed conformally over an exposed surface of said single-crystal region including over said PFET gate stack and said NFET gate stack.

[c29] The method of claim 28 further comprising stopping said recessing of said single-crystal region on said sides of said PFET stack and forming a second coating on said areas of said single-crystal region exposed by said recessing, and thereafter continuing said recessing, such that said second semiconductor does not grow in areas protected by said second coating.

[c30] The method of claim 29 further comprising growing a layer of said first semiconductor on said layer of said second semiconductor.

[c31] The method of claim 30 wherein said first semiconductor comprises silicon and said second semiconductor comprises silicon germanium, said silicon germanium having a germanium content of at least one percent.

[c32] The method of claim 29 wherein said second semiconductor applies said first strain as a compressive strain.